

REMARKS

The Applicants have carefully considered this Application in connection with the Examiner's Action, and respectfully request reconsideration of this Application in view of the foregoing amendment and the following remarks. The Applicants originally submitted Claims 1-43 in the Application. In response to a restriction requirement, the Applicants elected Claims 1-10, and withdrew Claims 11-43 from consideration pending the filing of a Divisional Application. The Applicants have now canceled Claims 1-10, without prejudice or disclaimer, and have added new Claims 44-53. Claims 44-53 do not recite new matter, support for the claims being in the specification, as filed. Accordingly, Claims 44-53 are currently pending in the Application.

I. Rejection of Claims 1, 2 and 7 under 35 U.S.C. §102

The Examiner has rejected Claims 1, 2 and 7 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,983,538 to Gotou. The Applicants have canceled Claims 1-10, and have added new independent Claim 44, from which Claims 45-53 depend. Claim 44 does not recite new matter, support being found throughout the specification, as filed. (See, for example, page 17, line 5, to page 18, line 9).

In contrast to independent Claim 44, Gotou discloses a MOSFET formed in a silicon carbide layer grown on a semiconductor wafer. (See column 1, lines 21-53). However, Gotou does not disclose a semiconductor device comprising a MOSFET having a silicon carbide tub located within or contacting a conductive substrate including a material different from the silicon carbide tub, in combination with a CMOS device formed on the conductive substrate where the CMOS device has a tub comprising the material. In fact, Gotou makes no mention of forming a MOSFET having a

silicon carbide tub, together with a CMOS device, in or contacting the same conductive substrate. As a result, Gotou does not anticipate independent Claim 44.

In conclusion, Gotou does not disclose each and every element of independent Claim 44, and, as such, is not an anticipating reference. Since Claims 45-53 depend from Claim 44, Gotou is also not an anticipating reference for Claims 45-53. Accordingly, the Applicants respectfully request the Examiner withdraw the §102 rejection with respect to any pending claims.

II. Rejection of Claims 3-6 and 8-10 under 35 U.S.C. §103

The Examiner has rejected Claims 3-6 and 8-10 under 35 U.S.C. §103(a) as being unpatentable over Gotou. As mentioned above, the Applicants have canceled Claims 1-10, and have added new independent Claim 44, from which Claims 45-53 depend.

In addition, as discussed above, Gotou does not disclose each and every element of new independent Claim 44. There is also no suggestion of these missing elements since Gotou is directed to forming one or more active devices on a silicon carbide layer, and makes no mention of a MOSFET having a silicon carbide tub within or contacting a conductive substrate along with a CMOS device formed in the same conductive substrate. As a result, one who is skilled in the art would find no motivation in Gotou to arrive at the semiconductor device recited in independent Claim 44.

In conclusion, Gotou does not teach or suggest the invention recited in independent Claim 44 and its dependent claims, when considered as a whole. As such, Gotou does not establish a *prima facie* case of obviousness of Claim 44 or Claims 45-53, which depend from Claim 44. Accordingly, the Applicants respectfully request the Examiner withdraw the §103 rejection with respect to any pending claims.

III. Conclusion

The Applicants respectfully request that the rejections be withdrawn and solicit a Notice of Allowance for Claims 44-53. The Applicants further attach hereto a marked-up version of the amendment made to the claims. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE
IN THE CLAIMS:

(1) Claims 1-10 have been canceled, without prejudice or disclaimer.

(2) The following new Claims 44-53 have been added:

44. A semiconductor device, comprising:
a lateral metal-oxide semiconductor field effect transistor (MOSFET), including:
a silicon carbide tub located within or contacting a conductive substrate including
a material different from the silicon carbide tub;
a gate formed on the silicon carbide tub; and
source and drain regions located in the silicon carbide tub and laterally offset from
the gate; and
complimentary metal-oxide semiconductor (CMOS) device formed on the conductive
substrate, the CMOS device having a tub comprising the material.

45. The semiconductor device as recited in Claim 44 wherein the MOSFET has a
breakdown voltage greater than an operating voltage of the CMOS device.

46. The semiconductor device as recited in Claim 44 wherein the MOSFET has a
breakdown voltage of at least about 10 volts and the CMOS device has a breakdown voltage
between about 3 volts and 5 volts.

47. The semiconductor device as recited in Claim 44 wherein the semiconductor device is a power converter and the MOSFET is a power switch for the power converter.

48. The semiconductor device as recited in Claim 44 wherein the silicon carbide tub is located within a trench formed in the conductive substrate.

49. The semiconductor device as recited in Claim 44 wherein the silicon carbide tub is located over the conductive substrate.

50. The semiconductor device as recited in Claim 44 wherein the material is doped silicon, wherein the silicon is doped with a p-type dopant or an n-type dopant.

51. The semiconductor device as recited in Claim 44 wherein the source and drain regions are doped with a p-type dopant or an n-type dopant.

52. The semiconductor device as recited in Claim 44 further comprising a buried oxide layer formed in the conductive substrate.

53. The semiconductor device as recited in Claim 44 wherein the conductive substrate comprises silicon and wherein the silicon carbide tub comprises a 3C silicon carbide.